# FPGA Based 64-Bit Low Power RISC Processor Using Verilog HDL

# Abstract:

RISC is a design philosophy to reduce the complexity of instruction set that in turn reduces the amount of power consumption, space, cycle time, cost and other parameters taken into account during the implementation of the design. The advent of FPGA has enabled the complex logical systems to be implemented on FPGA. The intent of this paper is to design and implement 64 bit RISC processor using FPGA Spartan 3E tool. This processor design depends upon design specification, analysis and simulation. It takes into consideration very simple instruction set. The momentous components include Control unit, ALU, shift registers and accumulator register. Power consumption reduced by designing clocking techniques.

**Tools used:**

**Xilinx 13.2**